What is claimed is:

1. An integrated circuit device comprising a pin for receiving a direct current voltage component signal, the device comprising:

a signal source for applying an alternating current signal to the pin;

a buffer for converting the alternating current signal into a digital signal; and

a digital detector for detecting a frequency of the digital signal and outputting a predetermined detection signal.

2. The device of claim 1, wherein the predetermined detection signal is activated when the frequency of the digital signal is greater than or equal to a predetermined frequency.

3. The device of claim 2, wherein the digital detector comprises a transistor for attenuating a component of the digital signal having a predetermined logic level when the digital signal is oscillated at a frequency greater than or equal to a predetermined frequency.

4. The device of claim 2, wherein the predetermined detection signal is a signal for setting predetermined functional modes.

5. The device of claim 1, further comprising:

a register chain for generating successive transfer signals according to the digital signal in response to a clock signal; and

a decoder for generating functional mode signals according to transfer signals in response to the predetermined detection signal.

6. The device of claim 5, wherein the register chain comprises registers for generating the transfer signals.

7. The device of claim 5, wherein the decoder generates the functional mode signals through a logical combination of the transfer signals.

8. An integrated circuit device comprising a pin for receiving a direct current voltage component signal, the device comprising:

differential amplifiers for comparing a direct current voltage component signal applied to the pin with a plurality of reference voltages and generating differential amplification signals; and

a decoder for generating at least one functional mode signal according to a logical combination of the differential amplification signals.

9. The device of claim 8, wherein the reference voltages are between a lowest voltage level of a plurality of high level voltages of the integrated circuit device and a highest voltage level of a plurality of low level voltages of the integrated circuit device.

10. An integrated circuit device comprising a pin for receiving a direct current voltage component signal, the device comprising:

a pin for receiving an alternating current signal;

a buffer coupled to the pin for converting the alternating current signal into a digital signal; and

a digital detector coupled to the buffer for detecting a frequency of the digital signal and outputting a functional mode signal for setting a mode of the device.

11. The device of claim 10, wherein the digital detector comprises a plurality of inverter stages responsive to a reference signal.

12. The device of claim 11, wherein each inverter stage comprises:

a PMOS transistor; and

an NMOS transistor coupled in series to the PMOS transistor, the NMOS transistor having a size smaller than a size of the PMOS transistor.

13. The device of claim 12, wherein the functional mode signal depends on the size of the NMOS transistor for pull-down.

14. The device of claim 10, wherein the functional mode signal is activated when the frequency of the digital signal is greater than a predetermined minimum frequency.

15. The device of claim 14, wherein the predetermined minimum frequency depends on a size of an NMOS transistor relative to a PMOS transistor in an inverter stage of the digital detector.